ADRIJA MUKHERJEE

ELECTRICAL AND COMPUTER ENGINEERING (M.S.)

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Education

M. S	Electrical and Electronics Engineering, University of Florida	GPA: 3.22/4.0	2023-2025 (expected)
B. Tech	Electronics and Communication Engineering, Meghnad Saha Institute of Technology, MAKAUT, India	GPA: 8.56/10.0	2017-2021 (awarded)

Skills

- **Design Tools:** Cadence Virtuoso, LT-SPICE, Silvaco ATLAS
- **Analysis Tools:** MATLAB, Verilog-A
- **Relevant Coursework:** Solid State Devices, VLSI-Circuits and Technology, Microfabrication Technologies, Nanodevices, Semiconductor Fabrication Technology, Future of Microelectronic Technologies, Modern Memory Devices
- **Programming:** C, Python, Java, VHDL, Perl
- **Other:** Microsoft Office 365 and English, Bengali & Hindi Languages

Projects

- **Design of 4x2 SRAM circuit using Cadence Virtuoso**
- **Analysis of Emerging Devices for Energy Efficient Applications**
  - Designed, simulated and analyzed Logic Gates, XOR, XNOR & ADDER circuits in LT-SPICE & MATLAB.
  - The power dissipation, delay and power-delay product of the circuits were studied over different device parameter variation, temperature variation and different supply voltage in the sub-threshold regime.
- **Ferroelectric Devices based Logic Circuits and Memory Design**
  - Analyzed the efficacy of the Ferroelectric Devices over Conventional MOSFETs for energy-efficient digital applications.
  - Simulated sub-20nm Negative Capacitance TFET and designed 6T-SRAM using MATLAB.
- **Machine Learning aided Reliability Analysis of Emerging FETs using Monte Carlo Simulations**

Industry Experience

- **ITC INFOTECH INDIA LTD.** — **Kolkata, India**

Associate IT Consultant — **August 2021 – July 2023**

  - Ensured that personal & private data in use are in compliance with the applicable data protection rules.
  - Mitigated the unauthorized acquisition of personal and private data within the organization.

- **DIRAC LAB, IIT ROORKEE** — **Roorkee, India**

Research Intern — **November 2021 – August 2022**

  - Simulated and analyzed the Logic Circuits of Ferroelectric Devices using HZO as the gate oxide.
  - Analyzed the reliability issues of the Ferroelectric Devices by adjusting the different body parameters.
  - Designed a Ferroelectric TFET based memory circuits using LT-SPICE.

Publications

1. **A. Mukherjee,** P. Debnath, D. Nirmal, M. Chanda, **"A new analytical modelling of 10 nm negative capacitance-double gate TFET with improved cross talk and miller effects in digital circuit applications",** Microelectronics Journal, Volume 133, 2023, 105689, ISSN 0026-2692, (https://doi.org/10.1016/j.mejo.2023.105689)
2. A. Karmakar, **A. Mukherjee**, S. Dhar, & M. Chanda, **"A junctionless dual-gate MOSFET-based programmable inverter for secured hardware applications using nitride charge trapping"**, 2022 IOP Publishing Ltd (https://doi.org/10.1088/1361-6641/ac92a3)
3. Ghosh, S., Saha, P., **Mukherjee, A.** et al. "**Analytical Modeling of Core–Shell Junctionless RADFET dosimeter of Improved Sensitivity**", Silicon 14, 9091–9102 (2022). (https://doi.org/10.1007/s12633-022-01690-y)
4. **A. Mukherjee**, P. Debnath & M. Chanda (2023) "**Machine learning-based output prediction of negative capacitance tunnel-FET**", IJE, (https://doi.org/10.1080/00207217.2023.2224077)
5. **A. Mukherjee**, B. Ray, D. Das, S. Bhattacharyya, P. Debnath and M. Chanda, "**Impact of Temperature on Circuit Performances of Junctionless MOSFET in Sub-threshold Regime**," 2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), 2020, pp. 1-5, (doi: 10.1109/VLSIDCS47293.2020.9179918)