A Low-Power Low-Noise Capacitive Sensing Amplifier for Integrated CMOS-MEMS Inertial Sensors

Deyou Fang and Huikai Xie
Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida 32611, USA
dyfang@ufl.edu, hkxie@ece.ufl.edu

ABSTRACT

This paper presents a low-noise CMOS capacitive sensing amplifier with power consumption as low as 1mW for monolithic CMOS-MEMS inertial sensors. Low-power operation is achieved by using an open-loop, two-stage amplifier topology with fully differential input/output and chopper stabilization. High chopping frequency (up to 2 MHz) and capacitance matching with optimal transistor sizing are used to maximize signal-to-noise ratio. Offsets due to the sensor and circuits are reduced by ac offset calibration and dc offset cancellation. A pseudo-resistor MOS-Bipolar device is used to establish a stable dc bias at the sensing electrodes with very low noise. All the electronics, except the capacitor for the low-pass filter following the demodulation, are integrated on the same chip with MEMS inertial sensors. A prototype accelerometer integrated with this circuit has been fabricated using the TSMC 0.35-µm CMOS process with 3.3-V power supply. Experimental results show that this interface circuit achieves a gain of 40 dB over the chopper frequency range of 50 kHz to 1 MHz, with an equivalent input offset of about 1 mV. The sensor offset is attenuated by the interface circuit by more than 26 dB.

KEY WORDS

Integrated accelerometer, low power, preamplifier, capacitive interface circuits, chopper stabilization, MEMS

1. Introduction

With their small size and low cost, micromachined inertial sensors have a wide range of applications in space, automotive, consumer electronics and biomedical areas. Both bulk micromachining and surface micromachining have been used to fabricate micromachined accelerometers. Bulk micromachining provides silicon-crystal silicon (SCS) microstructures and large proof mass for high resolution and robustness, but typically requires complicated fabrication steps and wire-bonding to an ASIC chip. Surface micromachining, on the other hand, provides integrated electronics but suffers from light mass and large temperature dependence [1]. A recently developed deep reactive-ion-etch (DRIE) CMOS-MEMS process combines the advantages of both bulk micromachining and surface micromachining, simultaneously providing integrated electronics and large SCS proof mass [2]. This process is employed to fabricate integrated monolithic 3-axis micromachined accelerometers and gyroscopes.

Interface circuitry is an important part of integrated inertial sensors. The design of interface circuits with high sensitivity, low noise and large dynamic range is very challenging. Prior interface circuit designs for capacitive sensing were mainly focused on high sensitivity and low electronic noise, but low power consumption has not been achieved. Most of them have a power consumption of tens of milliwatts [3][4][5]. However, in consumer and biomedical applications, low power operation is always a predominant requirement. For example, battery powered wireless sensors normally are required to consume at most hundreds of micro-watts for long-time operation [6]. So design of interface circuits with medium to high performance at very low power consumption is very important.

This paper presents a low-noise interface circuit with low power consumption (≤1mW) for a monolithic integrated microaccelerometer fabricated using the DRIE CMOS-MEMS process [2]. Continuous-time voltage amplifier architecture is used in this capacitive sensing interface circuit, where chopper-stabilization is applied to reduce 1/f noise and dc offset of the circuit. Low power is achieved by choosing an open loop, two-stage differential difference amplifier as the interface circuit. The sensor input-referred noise is minimized by employing high chopping frequency (up to 2 MHz) and the optimum capacitance matching technique introduced in [5]. Reduction of dc offset due to circuit mismatch and compensation of ac offset due to sensor position mismatch are realized by using a differential difference amplifier topology. Robust dc bias at the high-impedance sensing electrodes is established by a pseudo-resistor MOS-Bipolar device that has very high incremental resistance and introduces almost no noise and very small parasitic capacitance [7]. In addition, except the capacitor for the low-pass filter following the demodulation, no off-chip components are needed in this design.

The design with open-loop continuous-time architecture utilizing chopper-stabilization in [5] dissipates a power of 30 mW (6mA×5V), and also uses a big off-chip capacitor for its dc offset cancellation. Without a big off-chip capacitor for DC feedback, the design described in this paper achieves a low power consumption of about 1 mW (330μA×3.3V); sink current for bias circuit (80uA in this design) is not included. And at the same time, the dc biasing of the high impedance sensing nodes is greatly simplified by utilizing the MOS-Bipolar technique. With a folded-cascode linearized transconductance amplifier as the second stage, low voltage operation with good linearity and high output swing is also achieved.

In this paper, the topology for the low power, low noise interface circuit is introduced in Section 2. Section 3 gives the circuit design details. Experimental results of the interface circuit are presented in Section 4.

2. Topology of the Low-power, Low-noise Interface circuit

Both switched-capacitor (SC) charge integration method and continuous time voltage amplification with chopper-stabilization (CHS) are widely used in capacitive sensing [8]. Correlated double sampling (CDS) is often used in the former method to reduce dc offset and low frequency flicker noise; while chopper stabilization is applied in the latter method to reduce these circuit non-idealities [9]. At the same level of power consumption, the SC charge integration circuit for low capacitance sensing applications has higher noise floor due to high kT/C noise, thermal noise of MOS switches, and noise folding in sampled-data systems [5]. Because of the relatively small sensing capacitance (hundreds of fF to a few pF) in integrated CMOS-MEMS accelerometers, the chopper stabilization based continuous-time method is therefore chosen for the interface circuit to achieve low noise and low power simultaneously.

An open-loop, two-stage differential difference amplifier (DDA) operating in continuous time is applied as the interface circuit in this design. Block diagram of the interface circuit is shown in Fig. 1. Low power operation without performance degradation is achieved by a careful balance among the power consumption, noise, gain and linearity. In this topology, the first stage is optimized to achieve low noise, but at the same time provides a moderate gain (about 10). Since the sensing signal is very small (up to a few tens of mV), linearity will not be affected by the first stage. At the same time the sensor offset can be reduced in this stage with two extra tuning inputs. While for boosting the signal further, the second stage is also designed for high linearity and large output swing, so its gain can not be very high, which is normally in the range of 10 to 20. So, an overall gain of 100 to 200 (40~46dB) is achievable with this design.

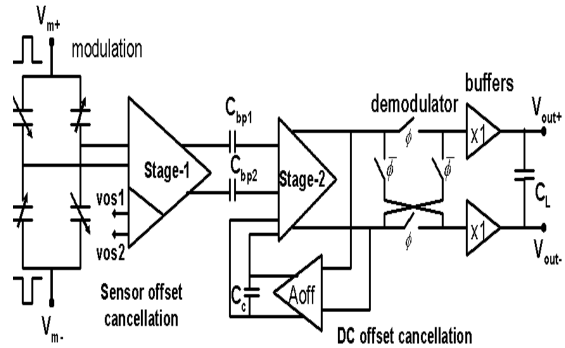


Figure 1. Topology of the low power, low noise capacitive sensing interface circuit.

Due to the small size of the input transistors in the first stage, which is used to maximize the signal-to-noise ratio, the dc offset at the output of the first stage may be fairly high (in tens of mV), so ac coupling between the two stages is used to cancel this offset. The output dc offset of the second stage is cancelled with a dc feedback, where a very narrow-band low pass g_m-C filter is applied in the feedback loop to reduce the dc offset, while the sensed signal at the chopping frequency will not be affected. Compared to the integrator-based continuous-time amplifier in [10], this topology can support high chopping frequency (in the range from 100 kHz to 2 MHz) with small sink current, therefore low power and low noise can be achieved simultaneously.

One of the design challenges for continuous-time capacitive sensing interface circuits is the robust dc bias of the high impedance nodes, which must have high ac impedance and small parasitic capacitance to achieve low noise and small signal attenuation. In previous designs, the sensing nodes have been biased by reverse-biased diodes, sub-threshold MOS transistors, long-channel MOS transistors, or large resistors [11][12][13][14]. Switched biasing of the sensing nodes is also used in [5], but it has the drawback of introducing charge injection and signal distortion [15]. In this design, the large resistance for dc biasing is implemented by using a pseudo-resistor MOS-Bipolar device introduced in [7].

As shown in Fig. 2, the MOS-Bipolar is a diode-connected PMOS transistor with the N-Well connected to the source. For a small size (W=1.0μm, L=0.5μm) PMOS transistor in such a configuration, an incremental resistance of 100 GΩ is achieved with an across voltage less than 0.4 V, and only a several fF parasitic capacitance is introduced.

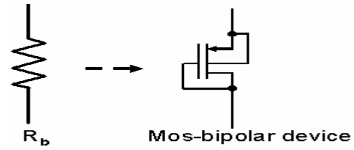


Figure 2. Implementation of dc bias.

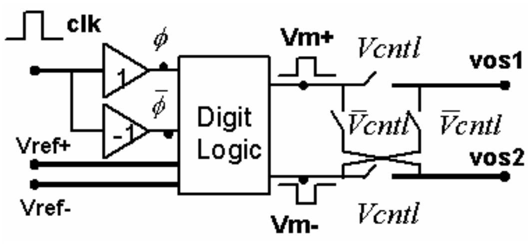


Figure 3. Circuit to generate modulation signal and signal for sensor offset cancellation.

The modulation signal is generated on chip with the main clock and two reference voltages, as shown in Fig. 3. The two dc reference voltages are used to set the amplitude of modulation signal applied to the full capacitive bridge of the sensing structure. Because the dc offset of the amplifier is effectively cancelled, a passive synchronous demodulator is used to recover the final acceleration signal, which consumes much lower power compared to a switched-capacitor demodulator such as used in [14].

To the interface circuit, the signal generated by the sensor offset is indistinguishable from the sensed dc acceleration signal. Furthermore, the sensor offset can be much larger than the sensing signal and even saturate the interface circuit. Therefore, calibration is needed for normal operation of the integrated microaccelerometer.

To overcome this problem, two extra inputs added in the first stage to calibrate the sensor offset, where the input signals for the calibration are generated from the modulation signals with the offset control signal V_{cntl}, as shown in Fig. 3. In the full capacitive bridge sensing configuration of the CMOS-MEMS accelerometer, the signal resulted from the sensor offset is either in phase or 180° out of phase with respect to the modulation signal. With the help of double-cross switches controlled by V_{cntl}, we can make the input signals for the sensor offset calibration either in phase or 180° out of phase to the signal generated by the sensor offset.

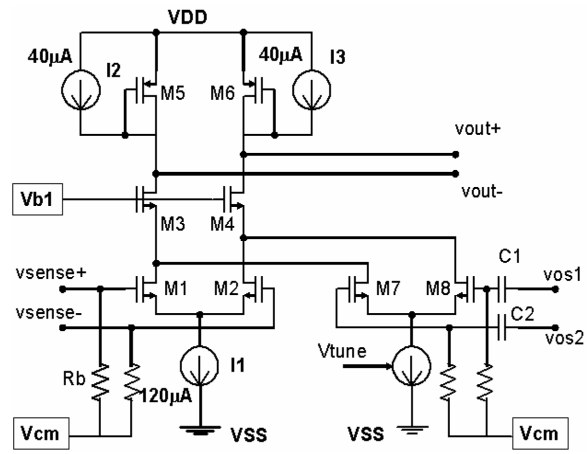


Figure 4. Schematic of stage-1.

3. Circuit Design

The schematic of the first stage of the interface circuit is shown in Fig. 4, where the above-mentioned pseudo-resistor MOS-Bipolar technique is used for the dc biasing. M3 and M4 are cascode transistors used to reduce Miller effect that will attenuate the effective gain if not reduced. A combination of a diode-connected transistor and a

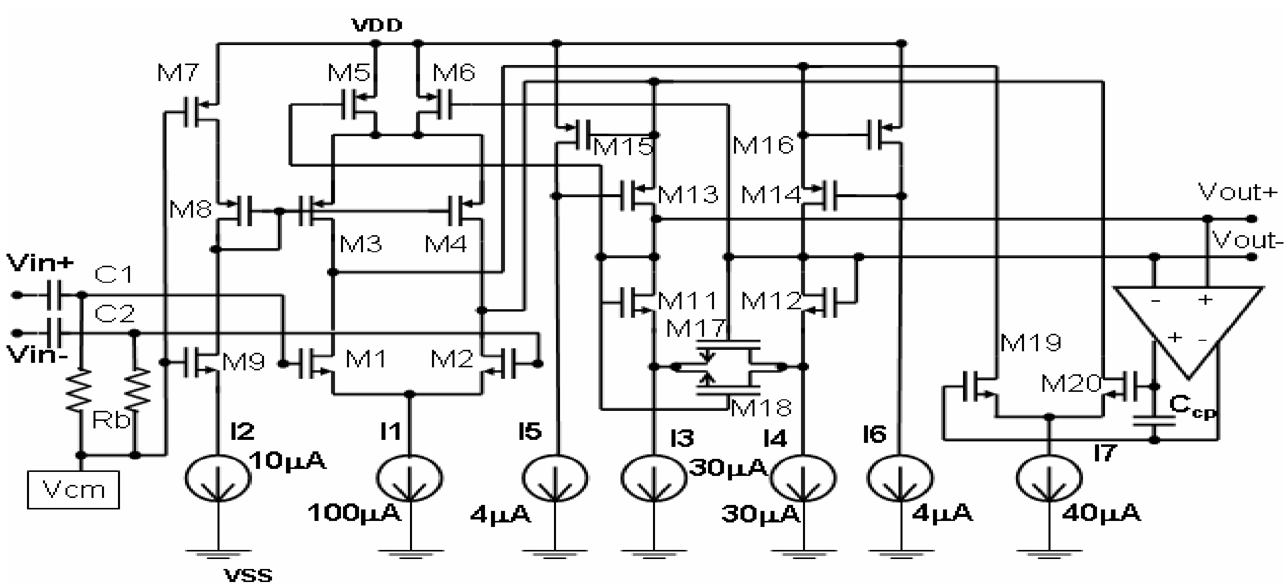


Figure 5. Schematic of stage-2.

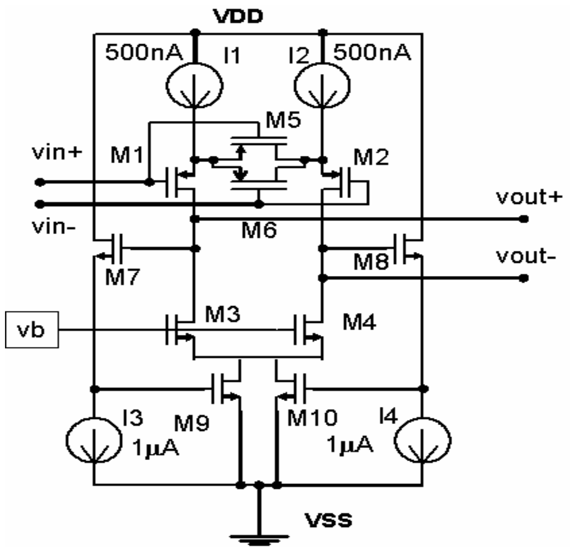
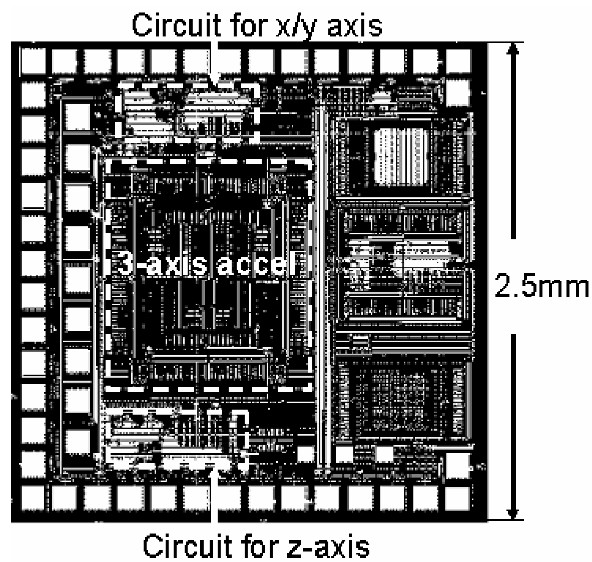


Figure 6. Schematic of fully-differential narrow-band OTA used in dc feedback loop.

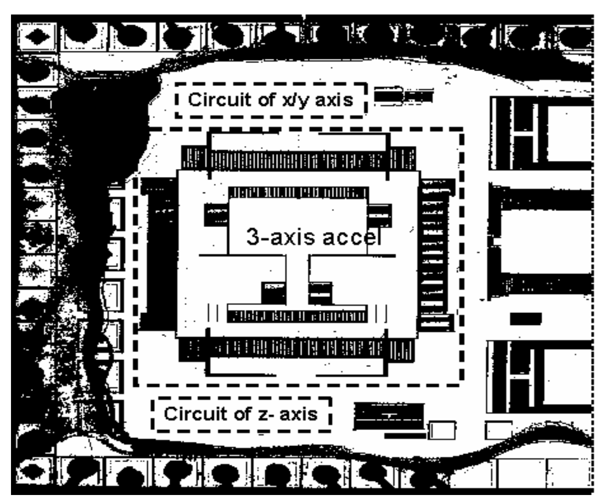
current source is used as the active load, which can achieve a higher gain without using a very small W/L ratio as in the pure diode-connected load configuration. To the first order, the gain is g_{m_1}/g_{m_5}. By reducing the bias currents of M5 and M6, g_{m5} can be effectively reduced; so the gain will be boosted accordingly. Another beauty of this configuration is that the offset due to the mismatch of the transistors has small effect on the gain. M7 and M8 are the extra pair of inputs for the sensor offset calibration. The input signals for calibration are generated on-chip with the modulation signal as stated in Section 2, which are attenuated by the capacitive voltage divider formed between the bypass capacitor and the C_{gs} of the input transistors for the offset cancellation. Off-chip V_{tune} is used to tune the sensor offset by controlling g_m of M7 and M8.

Low noise is achieved by using high chopping frequency (~2 MHz) and optimal sizing of the input transistors with respect to the sensing capacitance. N-MOS transistors are used for the input pair because they have low thermal noise while the flicker noise is minimized by the CHS technique. In addition, they also have low offset. Simulation shows that the first stage achieves a gain of 10 and contributes a noise floor of 15 $nV/\sqrt{Hz}$ with 1 MHz chopping frequency.

The schematic of the second stage is shown in Fig. 5. A folded cascode amplifier with linearized transimpedance load is applied to achieve good linearity and high output swing [16]. Within this stage, a DC feedback loop is utilized to cancel DC offset. In order to avoid using a large off-chip capacitor for the low pass g_m-C filter in the feedback loop, the offset amplifier must have a low g_m and high dc gain. A narrow-band fully-differential operational transconducatance amplifier (OTA) is designed for this low pass g_m-C filter, with its schematic shown in Fig. 6. In this narrow-band OTA, a PMOS input pair with source degeneration is used to achieve low g_m (in several μS). Meanwhile, the current source is applied as an active load to achieve a high gain. Transistors M7~M10 are used for common-mode feedback. M9 and M10 serve as a level shifter to bring the common-mode voltage of the offset amplifier outputs into the range that guarantees the dc feedback pair M19 and M20 (in Fig. 5) to work in the saturation region. With an on-chip 20-pF capacitor, the cutoff frequency of the low-pass filter is in tens of kHz, which allows a wide range of chopping frequencies (100 kHz to 2MHz).



(a) Layout of 3-axis accelerometer.



(b) Photograph of the tested chip.

Figure 7. (a) Layout of the 3-axis accelerometer, and (b) photograph of the tested chip.

With sensing capacitance of 200 fF, simulation results show that this interface circuit achieves a gain of 43 dB with the chopping frequency ranging from 100 kHz to 2 MHz. When chopped at 1 MHz, the total equivalent input noise is 24 nV/$\sqrt{Hz}$; the equivalent circuit dc offset is less than 100 μV, and the sensor offset attenuation is more than 40dB. The interface circuit sinks a current of 330μA, in which the current for the bias circuit is not included.

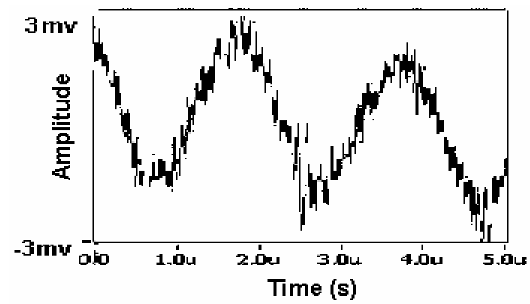
4. Experimental Results

A 3-axis CMOS-MEMS microaccelerometer integrated with this interface circuit has been fabricated with TSMC 0.35-μm technology with a 3.3-V power supply. The layout of the monolithic accelerometer and photograph of the tested chip are shown in Fig. 7(a) and Fig. 7(b) respectively, where the interface circuit takes an area of 300×600 μm^2, and size of the whole chip is 2.5×2.5 mm^2. The 3-axis accelerometer design and fabrication details is reported in [17]

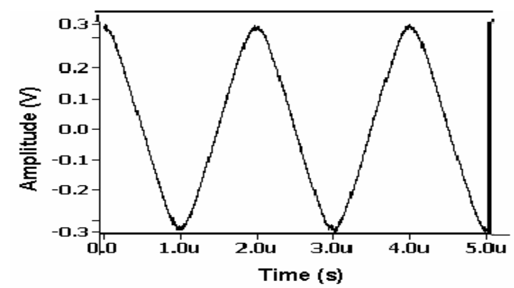
Due to the difficulty to generate square waves of very small amplitude (several mV), small sinusoidal test inputs are used instead. Fig. 8(a) and Fig. 8(b) show the input and output waveforms when a 500 kHz, 6 mV peak-peak sinusoidal test signal is applied. The waveforms are measured by Tektronix TDS 2014 oscilloscope, and extracted through Labview. It is obvious that a gain of 100 (before demodulation) is achieved. The experimental transfer function (before demodulation) with respect to the chopping frequency is plotted in Fig. 8(c), where a gain of 40 dB with chopping frequency ranging from 50 kHz to 1 MHz is achieved. The output dc offset of the interface circuit is 100 mV, which results in an equivalent input offset of 1 mV. Test results also show that the sensor offset can be reduced by more than 26 dB. Other parameters of the interface circuit and the whole integrated accelerometer are still under test.

5. Conclusion

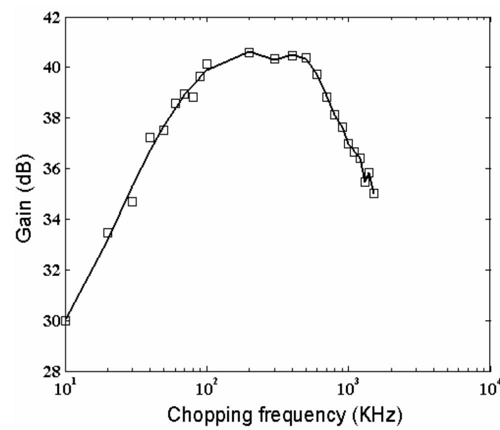
A low noise capacitive sensing interface circuit with power dissipation of 1 mW for the CMOS-MEMS integrated accelerometer is designed and fabricated. Simulation results shows that the circuit can achieve a noise level of 24 nv/$\sqrt{Hz}$ at chopping frequency of 1 MHz. Test results show that the circuit achieves a gain of 40 dB with chopping frequency ranging from 50 kHz to 1 MHz. An input circuit offset of 1 mV is achieved, and sensor offset is attenuated by more than 26 dB from experimental results.



(a) Input of test signal.



(b) Output of test signal.



(c) Gain vs. chopping frequency

Figure 8. Test results of interface circuit.

6. Acknowledgements

The authors acknowledge Hongwei Qu for device fabrication and wire bonding. This project is in part supported by the NASA UCF/UF Space Research Initiative. The authors thank the MOSIS Educational program.

References:

[1] N. Yazdi, F. Ayazi, and K. Najafi, Micromachined inertial sensors, *Proceedings of the IEEE, 86*(8), 1998,1640-1659

[2] H. Xie and G.K. Fedder, A DRIE CMOS-MEMS Gyroscope, *IEEE Sensors 2002 Conference*, Orlando, FL, 2002.

[3] M. Lemkin and B. E. Boser, A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics, *IEEE J. Solid State Circuits, 34*(4), 1999, 456-468.

[4] N. Yazdi, K. Najafi, An interface IC for a capacitive silicon µg accelerometer, *The IEEE International Solid-State Circuits Conference (ISSCC'99)*, 1999, 132-133.

[5] J. Wu, G. K. Fedder, L. R. Carley, A low-noise low-offset capacitive sensing amplifier for a 50-µg/$\sqrt{Hz}$ monolithic CMOS MEMS accelerometer, *IEEE Journal of Solid-State Circuits, 39*(5),2004,722-730.

[6] T.-H., Lin, H. Sanchez, R. Rofougaran, W. J. Kaiser, Micropower CMOS RF components for distributed wireless sensors; *The 1998 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,*1998, 157-160.

[7] R.R. Harrison, C. Charles, A low-power low-noise CMOS amplifier for neural recording applications, *IEEE Journal of Solid-State Circuits, 38*(6), 2003, 958-965.

[8] B. E. Boser, Capacitive interfaces for monolithic integrated sensors, *RF Analog-to-Digital Converters; Sensor and Actuator Interfaces; Low-Noise Oscillators, PLLs and Synthesizers* (Kluwer Academic Publishers, November 1997).

[9] C. C. Enz,, G.C. Temes, Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization, *Proceedings of the IEEE, 84*(11), 1996,1584 -1614.

[10] J. Geen, S. J. Sherman, J. Chang, and S. J. Lewis, Single-chip surface micromachined integrated gyroscope with 50°/hour Allan variance, *IEEE J. Solid-State Circuits, 37*(12), 2002, 1860-1866.

[11] ADXL05/50/105/202 Signal Chip Accelerometer With Signal Conditioning Datasheets, Analog Devices, Cambridge, MA.

[12] G. K. Fedder, Simulation of microelectromechanical systems, *Doctoral Dissertation, University of California at Berkeley*, 1994.

[13] G. Zhang, H. Xie, L. E. de Rosset, and G. K. Fedder, A lateral capacitive CMOS accelerometer with structural curl compensation, *12th IEEE Int. Conf. Micro Electro Mechanical System (MEMS'99)*, Orlando, FL, 1999, 606-611.

[14] H. Luo, G. Zhang, G. K. Fedder, and L. R. Carley, A post-CMOS micromachined lateral accelerometer, *J. Microelectromechan. Syst., 11*(3), 2002, 188-195.

[15] B.R. Schiffer, A. Burstein, W. J. Kaiser, An active charge cancellation system for switched-capacitor sensor interface circuits; *IEEE Journal of Solid-State Circuits, 33*(12), 1998, 2134-2138.

[16] C. Menolfi,, Q. Huang, A low-noise CMOS instrumentation amplifier for thermoelectric infrared detectors; *IEEE Journal of Solid-State Circuits, 32*(7), 1997, 968-976.

[17] H. Qu, D. Fang, H. Xie, Single-Crystal Silicon 3-axis CMOS-MEMS Accelerometer, *Proceedings of the 3rd IEEE Conference on Sensors*, Vienna, Austria, 2004